Lab 3 – Interference in the Memory System

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# Task 2: Baseline, Stat! (Again)

We can compute maximum slowdown as:

The weighted speedup can be computed as:

# Task 3: Way Partitioning

The base code emulates an 8-way memory structure. In order to modify this, we noticed that the list was a bounded list of lists, which themselves were bounded to objects in .

Our implementation strategy was simple – In order to add in core-locked ways *without* modifying the cache’s overall functionality, associativity, block sizing, set sizing, etc, and still reuse the base code, we cut down the number of ways to and duplicated the list of cache line sets by . This gave us -way associativity overall, where every set of ways was specified to a particular core, without changing the number of sets, block sizings, or any significant functionality.

This required us to change some of the function headers to ensure that core information would be passed down through various call chains such that proper eviction was possible.

Our way partitioning implementation was significantly fairer than the baseline implementation, receiving a much larger weighted speedup. However, the performance was significantly worse.

# Task 4: BLISS

We implemented BLISS by tracking information in the controller and utilizing that information to compare two requests in the scheduler.

Interestingly, we found that (by functional specification from the PDF) it was possible for all cores to be locked up with no memory access until the next cycle quanta. If one core performed requests back-to-back, it would be blacklisted, and the other cores were capable of sending requests much faster, increasing their chances of being blacklisted, etc. As such, the “blacklisting” part of BLISS would stop being relevant after three cores lock up – After the next consecutive requests from one core, all cores would be blacklisted, and would be served in a first-come first-serve basis until the start of the next cycle quanta (and the blacklisting would have no significant effect on performance).

# Task 5: A custom scheduler

The following are a series of graphs of all of our scheduling mechanisms, overlaid upon each other to compare performance.

## Equity scheduler

Our original idea was to evolve BLISS’s mechanism to better improve performance. In particular, having blacklists was an interesting idea to solve fairness, but as mentioned earlier, it did not significantly allow us to be “fairer” to threads – Instead, with two blacklisted threads or two non-blacklisted threads, it simply boiled down to first-come first-serve in most cases. Threads that were memory hogs would compete with other threads that were memory hogs quickly.

We wanted to take this blacklisting concept and flip it – That is, instead of deprioritizing memory hogs, inversely prioritize stingy threads that did not make many requests. This led to our implementation of equity scheduler, which computes the number of requests a thread would make and allows it access correspondingly. Any ties are still broken with first-come first-serve.

This resulted in a decent amount of performance, but it’s not as fair as way partitioning.

## Equitable BLISS scheduler

Our next idea was to leverage BLISS’s performance gains but still add another key of further incentivizing low usage to particular cores. As such, we implemented BLISS alongside our equity scheduler, with our equity scheduler being the tiebreaker for any BLISS operations and having FR-FCFS as our final tiebreaker.

The results of this showed improvements on our prior Equity scheduler overall,